Project #2

Simulation of CPU, Cache, Bus, and Memory Datapath

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**I. Executive Summary**

This report goes over what project the group was assigned with, how the group went about designing and implementing the project by making certain assumptions, backing up those assumptions with correct output data. The report finishes with a longer conclusion and all the related code attached.

**II. Introduction**

# Goal

The goal of this project is to build a VHDL simulation of a 32-bit version of the MIPS processor. The developed architecture is to include a CPU, cache, bus, and memory modules that emphasize the simulation of hit/miss and data-path cache scenarios for different types of instructions.

# Theoretical Background

**Cache:** In modern computing systems, accessing data directly from disk or memory is relatively time consuming or *expensive.* This could pose an issue if a set variables stored in memory are extensively required by the computing unit since accessing the respective variables could be time consuming. To deal with this, caches are utilized to minimize this overhead. Caches acts a less expensive intermediate storage block that stores blocks of memory that have been access, been accessed or are going to be accessed be the program.  If the requested data is in fact present contained in the cache a ***cache hit*** is identified, this request can be served by simply reading the cache, which is comparatively faster than accessing the memory. Otherwise, if the data block is not present a ***cache mis*s** is identified and the data has to be fetched from its respective location in memory. For efficiency, multiple caches are usually implemented to perform difference functions. Widely implemented abstractions usually involve the separation of cache into two main functions, *Instruction Cache* *and Data Cache.*

**Instruction Cache:** A stores instruction which helps in reducing the cost of going to memory to fetch instructions. In some other cases it also has other functions, such as branch prediction information. Instructions are only read/brought to the iCache and cannot be modified. So when the I-cache is full and a block of instructions is to be placed into the cache, it can usually over-write anywhere in the cache.

**Data Cache** is a intermediate storage component that contains the application data that is going to be utilized by the processor. Data is loaded from memory into the data cache. The element needed is then loaded from the cache line into a register and the instruction using this value can operate on it.

Along with different cache functions, there also exist different algorithms or *writing policies* that dictate the interaction between the cache and the memory. In this project’s case the chosen writing policy implemented was the ***Write Back with write Allocate*** policy which involves the following:

- Write to main memory whenever a write-hit is performed to the cache

- If a write misses, allocate a line in the cache for the data written.

# Group Specific Specifications

**Instructions**

The MIPS processor is to support the three instruction formats of R, I, and J, along with store word and load word. A table was provided in the project specifications that included all the instructions to be designed



As seen in the table, there is a custom set of instructions that are to be implemented, which is chosen based on the last digit of the student ID’. In this groups case, the 4th set (BNE LUI) was chosen. Another group specific specification was the writing policy, which in our case was set to Write Through with Write Allocate.

**Write Strategies:**

Both of our digits ended in 4, so we used the following write strategies based on the project 2 specifications.

Write Thru:



Figure 1: Write Thru

Write Allocate:



Figure 2: Write Allocate

**III. Design**

The group decided after lots of discussion to split all of the required pieces of structure into separate modules and then combine them into an overall dataflow. This allowed for each individual component to be thoroughly tested. The overall dataflow can be seen below as well as in the appendix.



Figure 3: Datapath design of cache/memory system

Based on the figure above, the black lines are mostly data lines, and the orange lines are control inputs for specific block. There are six main blocks where a majority of the functionality takes place.

The ICache block is 256-Byte word-addressable cache (implemented as a 64x32 array, 2048 bits) The cache is directly mapped from memory so the following formula was used to calculate the index of the cache.

(1)

This block takes in the Instruction Address (Program Counter) from the test bench program, as well as a flag, IHC, to test the different functionality of either an Icache Hit or Icache Miss. Since we implemented a write through policy, on a cache hit we take the word value from cache and update it to memory. Upon a instruction miss in cache, the data will be fetched from memory. Since the Write Allocate strategy was implemented, a block of memory was put back in the cache to update it. The data is then correct and outputted. The mux on the top is to select either from the memory (ICache Hit) or from the cache after a block update (ICache Miss). The access time for the ICache operation is just 1 cycle (10 ns).

The Bus block is simply to model the bus delay. Since the specifications of the bandwidth of the bus stated, 32 words/cycle, the assumption was made that the bus will delay a full cycle when 32 words or less are put on the bus. Since the most that will put across the bus is a memory block (8 words) this assumption works.

The memory Block is 1024 Bytes of Byte-addressable storage (implemented as a 1024x8 array). The memory then has addresses from 0x0 to 0x3FF. When there is an ICache Hit, a word is brought into the memory to perform a word update, when there is an ICache Miss the Block of memory at the inputted address is outputted and write allocated back to cache to update the values in cache. After the correct instruction is retrieved from either the cache or memory, the Op-Code is inputted into the CPU Block. The memory has a port access time of 5 cycles/word for reads, and an additional memory read time of 3 cycles/word for a total of 8 cycles/word for reading. The memory has a port access time of 3 cycles/word for writes, and an additional memory write time of 4 cycles/word for a total of 7 cycles/word for writing.

The CPU is a simple block, based on the Op-code inputted from the instruction cache/memory process it will determine a couple output signals. The instructions that needed to be implemented are shown below:

|  |  |
| --- | --- |
| Common Name | Register Names |
| lw $s1, 200 ($t3) | lw R17,200(R11) |
| sw $s3, 100 ($t4) | sw R19,100(R12) |
| add $s3, $t3, $t2 | add R19,R11,R10 |
| beq $s5, $t6, 400 | beq R21,R14,0[400-PC] |
| bne $s5, $t6, 500 | bne R21,R14,0[500-PC] |
| lui $s6, 40 | lui R22,40 |

Table 1: Instruction Implemented

There are two types of instructions implemented ALU/Branch Instructions and Memory Access functions. The last four on the list above are the ALU/Branch instructions. These only require the use of register values. The Op-codes are determined to match specific instructions. For the beq and bne instructions in the CPU the ALU\_DONE flag will be set. For the other two, the register value will be updated with the proper value (add, lui). The Initial values of the register can be seen below.

|  |  |  |  |
| --- | --- | --- | --- |
| Register Number | Initial value | Register Number | Initial value |
| Reg 8 | 0x00000008 | **Reg 17** | 0x00000017 |
| Reg 9 | 0x00000009 | **Reg 18** | 0x00000018 |
| Reg 10 | 0x00000010 | **Reg 19** | 0x00000019 |
| Reg 11 | 0x00000011 | **Reg 20** | 0x00000020 |
| Reg 12 | 0x00000012 | **Reg 21** | 0x00000021 |
| Reg 13 | 0x00000013 | **Reg 22** | 0x00000022 |
| Reg 14 | 0x00000014 | **Reg 23** | 0x00000023 |
| Reg 15 | 0x00000015 | **Reg 24** | 0x00000024 |
| Reg 16 | 0x00000016 | **Reg 25** | 0x00000025 |

Table 2: Initial Register Values

This will give the following results for the Add and LUI.

|  |  |
| --- | --- |
| Register Names | Results |
| add R19,R11,R10 | R19 <= 0x00000021 |
| lui R22,40 | R22<= 0x00280022 |

Table 3: ALU Instruction Outputs

These two instructions, like the branch instructions will output the ALU\_DONE flag to signal that this branch is complete. For Load Word the ALU calculates the Data Address, sets the R\_W flag to 1 to signal a read, D\_Type flag to signal for the data memory access, and finally the Register number where the data in the memory will be loaded into the register. For Store Word the ALU calculates the Data Address, sets the R\_W flag to 0 to signal a write, D\_Type flag to signal for the data memory access, and the data in Register 19 (which is initially 0x19).

The DCache datapath will only be run through when there is a data memory access. This is only for the instructions Load word and Store Word, and signaled from the CPU as the D\_Type signal. The DCache block is 128-Byte word-addressable cache (implemented as a 32x32 array). The cache is directly mapped from memory so the following formula was used to calculate the index of the cache.

(2)

Once the correct value of the block is reached on a read hit (DCache Hit and Load Word), it will update the word in memory and output that data at the memory address, finally updating the value in the register file. On a read miss (DCache Miss and Load word), it will find the correct value in memory, and write allocate a memory block back to the DCache, updating 8 words in the DCache. On a write hit (DCache Hit and Store Word), the DCache will write Data value output from the ALU to the DCache, then it will be updated in memory. On a write miss (DCache Miss and Store Word), the DCache will store the correct value in memory, and then write allocate a block of memory back to the DCache.

**IV. Implementation**

To show the implementation of the cache/memory system, code snippets will be shown in respect to their programs. Most everything related specific values in the cache and memory were hardcoded; it made the process of debugging a lot simpler. In order to run through the entire memory sub systems the testbench was written to initialize the Instruction addresses and the Cache Hit types.

The ICache is 256-Bytes of word-addressable memory; this was achieved by using an array. It has inputs of an Instruction Address, the IHC flag, and a Block Input for write allocate. It outputs the data at the instruction address. An array was utilized to define the memory, and all the values were initialized to 0’s.

**type** i\_array\_type **is** **array** **(**0 **to** 63**)** **of** std\_logic\_vector**(**31 **downto** 0**);**

**signal** I\_Cache **:** i\_array\_type **:=** **((others** **=>** **(others=>**'0'**)));**

The memory is a direct map to the cache, equation 1 was used to index into the instruction cache array. In this component, if the IHC was asserted, modeling a hit, then the Op-codes would be defined at the address specified. And then the data would be outputted after 1 cycle time to model its access time. If the IHC was not asserted then it would check if a block was being inputted. Upon a miss, one goes to the memory and retrieves the block of memory and write allocates it back into the cache.

The DCache is 128-Bytes of word-addressable memory; this was achieved by using an array. It has inputs of the Data Address, the DHC flag, Data input, block input, a read/write signal. It also has an input to determine if the CPU found a ALU instruction or a memory instruction, this is done using an ALU\_Done flag. The Data Cache outputs LW and SW done flags as well as the data at the memory address. Like the ICache, an array was used to simulate the array. This can be seen below.

**type** array\_type **is** **array** **(**0 **to** 31**)** **of** std\_logic\_vector**(**31 **downto** 0**);**

**signal** D\_Cache **:** array\_type **:=** **((others** **=>** **(others=>**'0'**)));**

The memory is a direct map to the cache, equation 2 was used to index into the data cache array. In this component the code will only be ran if it is a memory instruction (Ie. ALU\_Done is set to 0). This ensures that no data is corrupted in the D-cache dataflow. The Read/Write signal is used to determine if the instruction was a load or store. When R/W is asserted a load instruction is being implemented. On a D-Cache hit, a fake value of x”77777777” is loaded into cache and then outputted to update memory. On a miss, it will go to memory and fetch a block of memory and write allocate it back into the cache. When the Read/Write signal is not asserted, meaning a store instruction is being implemented, on a D-Cache hit; the inputted data value will be stored to the cache and then outputted to update memory. On a D-Cache miss, it goes to memory to get a block to write allocate back to the D-Cache.

The memory module was modeled using an array. It is 1024 Bytes of word addressable. It has all the same inputs, the cache flags, R/W flag, and the address and the data that will update the word upon a hit. It then out puts the data at the memory and/or a block of memory. The array initialization can be seen below.

**type** array\_type **is** **array** **(**0 **to** 1023**)** **of** std\_logic\_vector**(**7 **downto** 0**);**

**signal** memory **:** array\_type **:=** **((others** **=>** **(others=>**'0'**)));**

When there is an instruction hit, the data will be brought in from the cache for the write through strategy. In the following definition C\_Type define which cache is being used, 0 for Instruction Cache, and 1 for Data Cache. This is done by the following code.

**if** **(**IHC **=** "1" and C\_type **/=** "1"**)** **then**

memory**(**mem\_blk**)** **<=** Data\_In**(**31 **downto** 24**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**1**)<=** Data\_In**(**23 **downto** 16**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**2**)** **<=** Data\_In**(**15 **downto** 8**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**3**)** **<=** Data\_In**(**7 **downto** 0**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

Since in memory has specified access times for read and write. In this case for the write through, it will take 3 Cycles/word for port access then an additional access time of 4 Cycles/word. This leads to 7 cycles/word. For this branch it will take 7 cycles to complete the writing to the memory. This strategy of delaying is used throughout all of the modules to model delay in the circuit. When there is a miss in either the data cache or the instruction cache this module will output a block of memory. It is specified that a block is 8 words, so when there is a read or write the delay times will be multiplied by 8 to account for the 8 separate words.

One of the simpler modules was the modeling the bus. The bus will just output whatever is inputted. Within the module, there is availability to input all the signals that have been described before, however the most important ones are a data word, and a block (8 words). These would just delay one cycle time and then outputted.

The CPU model is a highly simplified version of a typical CPU. In our case, since we are mainly modeling the cache/memory design, we simplified the CPU quite a bit. The CPU will just take in the Op-Code from the instruction cache/memory system. From the Op-code it determines a few key outputs, if it is an ALU instruction, it will set the ALU\_Done flag to 1 to signify the ALU operation is done. For the Memory functions, load and store, it will output the respective R/W signal, and the Data Address that was hardcoded (this was done since it was assumed that Register values were initialized and were constant at the each of the instruction). For the Load instruction the following code is used.

**if** **(**OPC **=** x"8D7100C8"**)** **then** --Load instruction

**report** "In load"**;**

ALU\_DONE**<=**"0"**;**

DAddr**<=**x"000000D9"**;** --200 + $11

R\_W**<=**"1"**;**

Data**<=**"1"**;**

Data\_reg**<=**x"00000000"**;**

Reg\_Num **<=** "10001"**;** --R17

One of the last modules that was created was the Register Data component. This simply initializes the register values, and inputs register number from CPU, and data input. For the Add and LUI this is where the Register Values will show being updated. And when the load instruction is inputted, it will load the data value into the specific register.

Once all of the modules were constructed and tested individually, they were combined into two major modules. In order to make the combination of the entire dataflow simple, the modules was split in two. The first one constructed was the ICache\_Dataflow that constructed the top half of the Figure showed in the Overall Data flow. This included the ICache, Bus, Memory, a Mux, and finally the CPU. The second one constructed was the DCache\_Dataflow that constructed the bottom half of the Figure shown in the Overall Data flow. This included the DCache, Bus, Memory, a Mux. These two modules were then constructed together along with the register file to obtain the final Testbench program, which we called Cache\_Memory\_Dataflow. This simple inputs the Instruction address, and the hit flags. It will then out the Done flags, and then finally the data out. When running the program, the register file can also be shown to show the register value changes.

**V. Results**

To test the implementation of the six instructions, different variables were plugged in the testbench and the respective waveforms were recorded. Below is a sample of some of the results obtained for 2 of the ALU operations (Add,LUI), a load, and a store operation. To ensure that the dChace and the iCache were functioning correctly, different iCache/dCache hit miss combinations were tested across ALU and non-ALU instructions as seen in the following table:

|  |  |  |
| --- | --- | --- |
| iCahce | dCache | Instruction tested |
| Hit | \* | Add(ALU) |
| Miss | \* | LUI(ALU) |
| Hit | Hit | LW |
| Hit | Miss | SW |

Table 4: Instructions Tested

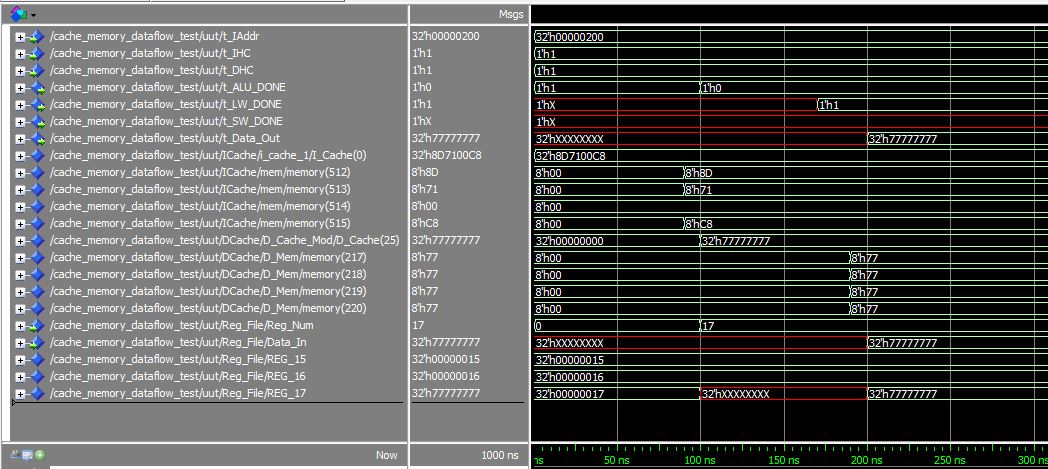
**Load**

|  |  |  |
| --- | --- | --- |
| Instruction Address | Instruction stored | Opcode |
| 0x200 | lw $s1, 200 ($t3) | 0x8D7100C8 |

Table 5: Load Instruction Test

**Test when iCache hit and dCache hit**:

The instruction load word is meant to load the word stored at 200($11) and store it in t3 (Reg 17).The following waveform was obtained by the test bench

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The waveform shows the following signals:

* **iAddr (instruction address)**: This input is set to 0x200 which is the hardcoded address for our load instruction
* **IHC (instruction hit flag):** This input is set to 1 to denote a iCache Hit
* **DHC (data hit flag):** This input is set to 1 to denote a dCache Hit
* **LW\_DONE:** set to high denoting that CPU has recognized the Load instruction
* **Data\_out:** set to 0x77777777 which shows the data stored at the location 200($11)
* **Reg\_17:** shows how the data loaded from memory stored in the destination $s1 or Register 17 i.e the success of the simulation

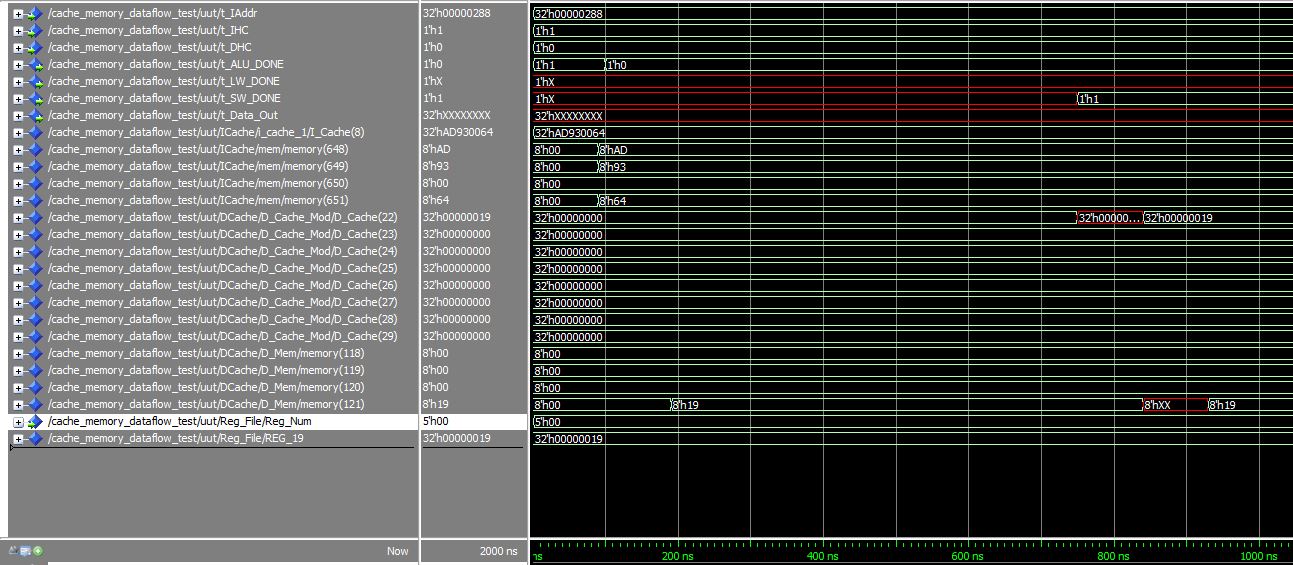
**Store**

|  |  |  |
| --- | --- | --- |
| Instruction Address | Instruction stored | Opcode |
| 0x288 | sw $s3, 100 ($t4) | 0xAD930064 |

Table 6: Store Instruction Test

**Test when iCache hit and dCache miss**

The instruction Store word is meant to store the word at $s3(Reg[19]) to the memory location designated by 100($t4).

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The waveform shows the following signals:

* **iAddr (instruction address)**: This input is set to 0x288 which is the hardcoded address for our store instruction
* **IHC (instruction hit flag):** This input is set to 1 to denote a iCache Hit
* **DHC (data hit flag):** This input is set to 0 to denote a dCache Miss
* **SW\_DONE:** set to high denoting that CPU has recognized it is a store operation
* **Reg\_19:** shows the data to be stored to memory stored in the destination memory
* **Memory\_121:** The destination memory shows 0x19 (the data from reg 19 ) stored i.e the success of the simulation

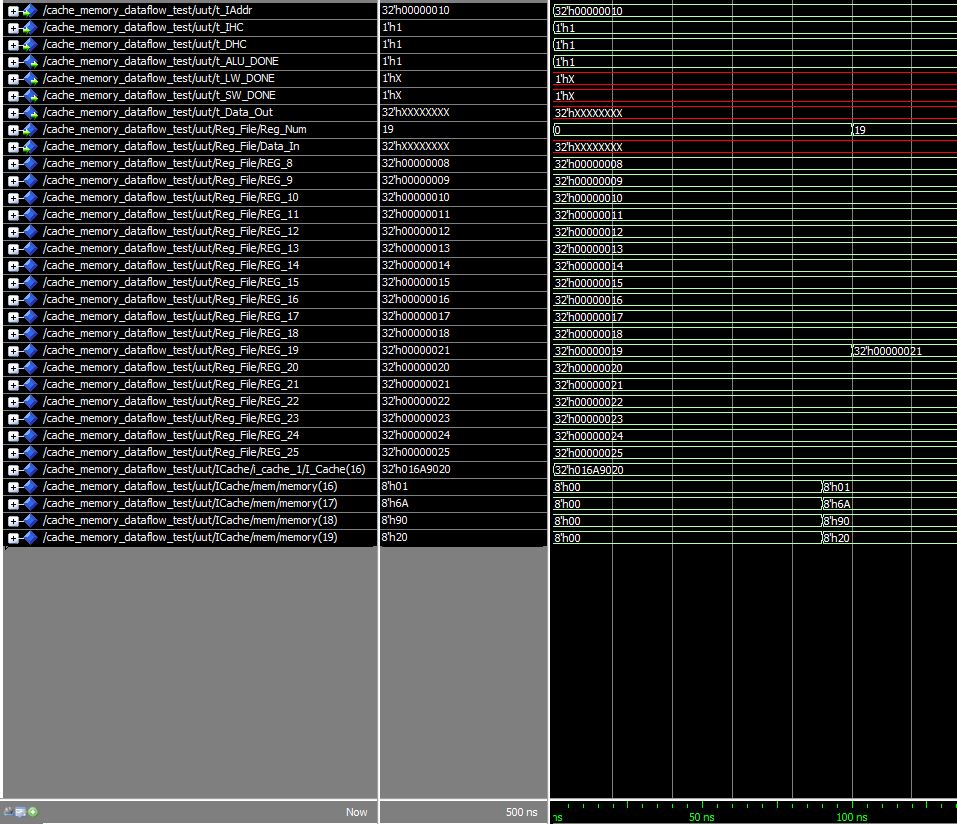
**Add**

|  |  |  |
| --- | --- | --- |
| Instruction Address | Instruction stored | Opcode |
| 0x010 | add $s3, $t3, $t2 | 0x016A9020 |

Table 5: Load Instruction Test

Adds two registers (Reg[10] and Reg[11]) and stores the value in 19. In our module this is an ALU operation and hence should assert the ALU\_DONE signal.

**Test when iCache hit and dCache hit**

****

The waveform shows the following signals:

* **iAddr (instruction address)**: This input is set to 0x010 which is the hardcoded address for our add instruction
* **IHC (instruction hit flag):** This input is set to 1 to denote a iCache Hit
* **ALU\_DONE:** set to 1 denoting that CPU has recognized it is a ALU operation
* **Reg\_10:** shows the value stored in register 10 which is set to 0x10
* **Reg\_11:** shows the value stored in register 11 which is set to 0x11
* **Reg\_19:** shows the value stored in register 19 which was at 0x19 at the beginning of the program and then was set to 0x21 (the summation of Reg\_10 and Reg\_11) which denotes a successful simulation of the instruction

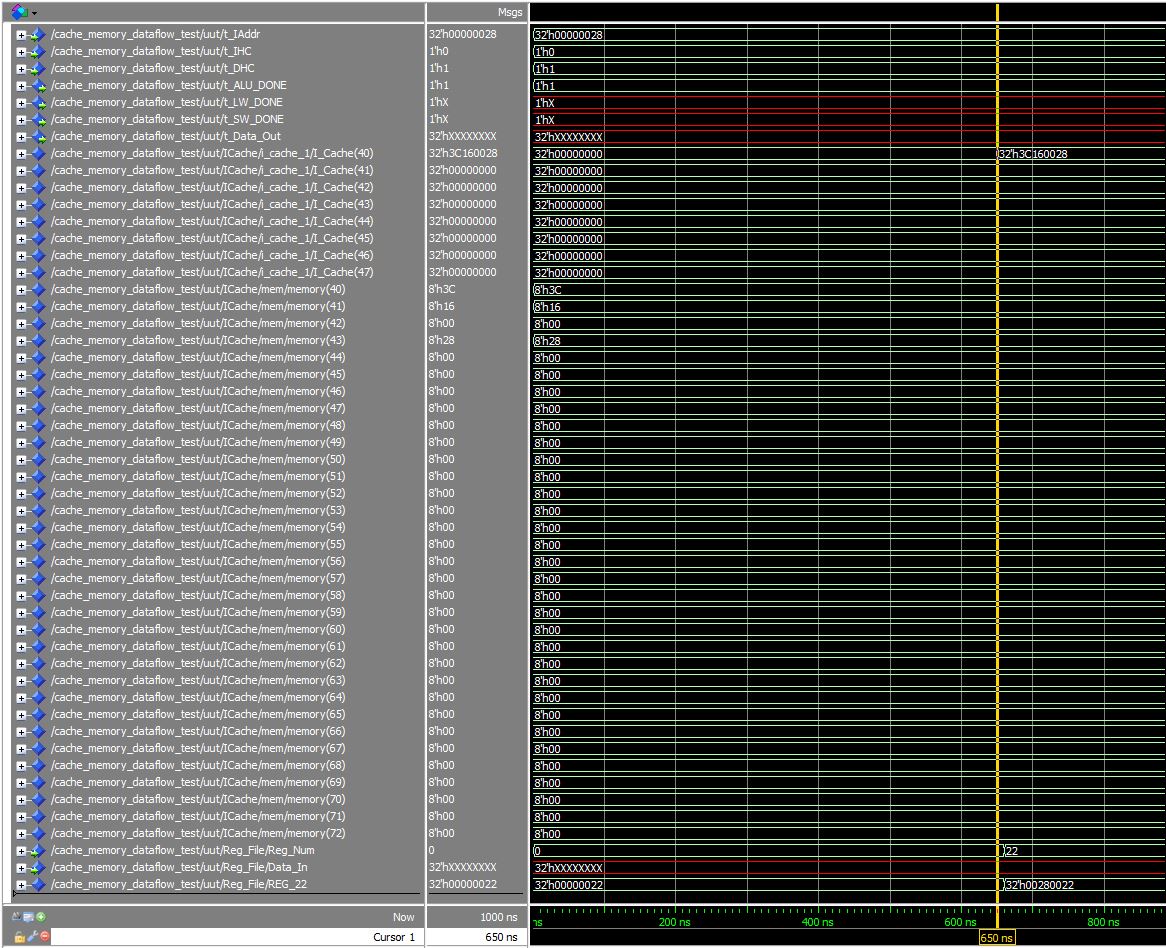
**Load upper immediate**

|  |  |  |
| --- | --- | --- |
| Instruction Address | Instruction stored | Opcode |
| 0x028 | **lui $s6, 40** | 0x3C160028 |

Table 6: LUI Instruction Test

The immediate value is shifted left 16 bits and stored in the register. The lower 16 bits are zeroes. The immediate value 40 is shifted 16 bits and stored in $s6 Reg[22]

**Test when iCache miss and dCache hit**

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* **iAddr (instruction address)**: This input is set to 0x028 which is the hardcoded address for our lui instruction
* **IHC (instruction hit flag):** This input is set to 1 to denote a iCache Hit
* **ALU\_DONE:** set to 1 denoting that CPU has recognized it is a ALU operation
* **Reg\_22:** shows the value stored in register 22 which was at 0x2 at the beginning of the program and then was set to 0x280022 which represent 40(0x28) shifted by 16 bits and appended to the register denotes a successful simulation of the instruction

**VI. Discussion**

The waveforms obtained are consistent with the expected behavior and thus represent a successful implementation of the modules.

In terms of development, the process went very smoothly and no major bugs were hard to deal with. This could primarily be attributed to the Object Oriented programming approach and testing techniques the team implemented. Writing simple component entities with specific tasks and then writing a test bench for each separate entity has definitely made the debugging process easier. The present code structure is also very scalable; having the separated modules facilitates the accommodation of any code feature addition/improvement in the future.

Even though this is probably outside the scope of the project specification, some nice future work could include deprecating some of the hardcoded instruction opcodes functionality, instead we can have the CPU get the instruction opcode, look it in a dictionary and ultimately be able to actually decode the instruction machine code rather than dealing with the hardcoded hex value.

**VII. Conclusions**

In conclusion, the developed code was successful in meeting the specifications. With hardcoding everything, the group knew what values would appear, and what each instruction would do. Knowing it all made everything a little bit easier to code. The report shows how each component was set up and how it all came together at the end in the final test bench program. The lab served as a good practical simulation for the expected workflow and ultimately provided the team with a more hands-on insight in respect to the operation of caches.

**VIII. Attachments**

Each individual program’s code will be attached, the individual test benches for the components won’t be necessary, since the overall test bench works without issue.

**ICache:**

--I-Cache: 256 Bytes (Word Aaddressable)

--Access time: 1 cycle

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** IEEE**.**NUMERIC\_STD**.all;**

**entity** I\_Cache **is**

**port** **(**IAddr **:** **in** std\_logic\_vector**;** --Instruction address

IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

Blk\_In**:** **in** std\_logic\_vector**(**255 **downto** 0**);** --Block size of 8 words

I\_Cache\_Data**:** **out** std\_logic\_vector**(**31 **downto** 0**));** --Data output of 32-bit memory

**end** **entity** I\_Cache**;**

**architecture** behave **of** I\_Cache **is**

--initialaztion of a memory array of 256 byte (word addressable 32bit data

**type** i\_array\_type **is** **array** **(**0 **to** 63**)** **of** std\_logic\_vector**(**31 **downto** 0**);**

**signal** I\_Cache **:** i\_array\_type **:=** **((others** **=>** **(others=>**'0'**)));** --Initialize everything to 0

**signal** temp **:** integer**;**

--signal mem\_blk : natural;

**shared** **variable** mem\_blk **:** natural**;**

--Address in cache for the instructions

**constant** lw\_addr **:** integer **:=** 0**;** --504-600 --0x200 (512)

**constant** sw\_addr **:** integer **:=** 8**;** --604-700 --0x288 (648)

**constant** add\_addr **:** integer **:=** 16**;** --0-500 --0x010 (16)

**constant** beq\_addr **:** integer **:=** 24**;** --0-500 --0x018 (24)

**constant** bne\_addr **:** integer **:=** 32**;** --0-500 --0x020 (32)

**constant** lui\_addr **:** integer **:=** 40**;** --0-500 --0x028 (40)

--Cycle Time Constant

**constant** cycle\_time **:** time **:=** 10 ns**;**

**begin**

ICache\_Proc **:process** **(**IAddr**,** IHC**,** Blk\_In**)**

**begin**

mem\_blk **:=** **to\_integer(**unsigned**(**IAddr**))** mod 64**;**

temp **<=** mem\_blk**;**

**if(**IHC **=** "1"**)** **then**

--Simulation of a I-Cache hit, Init OPC to already be in the cache

I\_Cache**(**lw\_addr**)** **<=** x"8D7100C8"**;**

I\_Cache**(**sw\_addr**)** **<=** x"AD930064"**;**

I\_Cache**(**add\_addr**)** **<=** x"016A9020"**;**

I\_Cache**(**beq\_addr**)** **<=** x"12AE0178"**;**

I\_Cache**(**bne\_addr**)** **<=** x"16AE01D4"**;**

I\_Cache**(**lui\_addr**)** **<=** x"3C160028"**;**

**elsif(**IHC **=** "0"**)** **then**

**if** **(**Blk\_In**(**255**)** **/=** 'U'**)** **then** --only does blk replacment when a blk\_in is inputed

--Simulation of a I-Cache miss, will write a blk into cache, write allocate

I\_Cache**(**mem\_blk**)** **<=** Blk\_In**(**255 **downto** 224**);**

I\_Cache**(**mem\_blk **+** 1**)** **<=** Blk\_In**(**223 **downto** 192**);**

I\_Cache**(**mem\_blk **+** 2**)** **<=** Blk\_In**(**191 **downto** 160**);**

I\_Cache**(**mem\_blk **+** 3**)** **<=** Blk\_In**(**159 **downto** 128**);**

I\_Cache**(**mem\_blk **+** 4**)** **<=** Blk\_In**(**127 **downto** 96**);**

I\_Cache**(**mem\_blk **+** 5**)** **<=** Blk\_In**(**95 **downto** 64**);**

I\_Cache**(**mem\_blk **+** 6**)** **<=** Blk\_In**(**63 **downto** 32**);**

I\_Cache**(**mem\_blk **+** 7**)** **<=** Blk\_In**(**31 **downto** 0**);**

**end** **if;**

**end** **if;**

**end** **process** ICache\_Proc**;**

--Output The opcode

I\_Cache\_Data **<=** I\_Cache**(to\_integer(**unsigned**(**IAddr**))** mod 64**)** **after** cycle\_time **when** **(**IHC **=** "1"**)** **else** --If hit

I\_Cache**(to\_integer(**unsigned**(**IAddr**))** mod 64**)** **after** cycle\_time **when** **(**IHC **=** "0" and Blk\_In**(**255**)** **/=** 'U'**);**

--Blk\_In(255 downto 224) after cycle\_time when (IHC = "0" and Blk\_In(255) /= 'U');

**end** **architecture** behave**;**

**DCache:**

--D\_Cache: 128 Bytes (Word Aaddressable)

--Access time: 1 cycle

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** IEEE**.**NUMERIC\_STD**.all;**

**entity** D\_Cache **is**

**port** **(**DAddr **:** **in** std\_logic\_vector**;** --Data address

DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 bit DCache Flag Input (1 for hit, 0 for miss, given by testbecnh)

Data\_In **:** **in** std\_logic\_vector**(**31 **downto** 0**);** --32-bit data in

Blk\_In**:** **in** std\_logic\_vector**(**255 **downto** 0**);** --Block size of 8 words

R\_W **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 for load, 0 for store

ALU\_Done **:** **in** std\_logic\_vector **(**0 **downto** 0**);** --1 for done, 0 for not done

LW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**);** --1 for done, 0 for not done

SW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**);** --1 for done, 0 for not done

D\_Cache\_Data**:** **out** std\_logic\_vector**(**31 **downto** 0**));**--data output of 32-bit memory

**end** **entity** D\_Cache**;**

**architecture** behave **of** D\_Cache **is**

--initialaztion of a memory array of 128 byte (word addressable 32bit data

**type** array\_type **is** **array** **(**0 **to** 31**)** **of** std\_logic\_vector**(**31 **downto** 0**);**

**signal** D\_Cache **:** array\_type **:=** **((others** **=>** **(others=>**'0'**)));** --Initialize everything to 0

**shared** **variable** mem\_blk **:** natural**;**

--Address positions

**constant** cycle\_time **:** time **:=** 10 ns**;**

**begin**

DCache\_Proc **:** **process** **(**Daddr**,** DHC**,** R\_W**,** ALU\_Done**,** Blk\_In**)**

**begin**

mem\_blk **:=** **to\_integer(**unsigned**(**DAddr**))** mod 32**;**

--Not an alu operation -> SW or LW

**if** **(**ALU\_Done **=** "0"**)** **then**

--Load Hit

**if** **(**DHC **=** "1" and R\_W **=** "1"**)** **then**

--Fake cache inililzation

D\_Cache**(**mem\_blk**)** **<=** x"77777777"**;** --Fake Data at cache address

LW\_Done **<=** "1"**;**

--Load Miss

**elsif** **(**DHC **=** "0" and R\_W **=** "1"**)** **then**

**if** **(**Blk\_In**(**255**)** **/=** 'U'**)** **then** --Only does the blk replacment if a Blk is inputed

D\_Cache**(**mem\_blk**)** **<=** Blk\_In**(**255 **downto** 224**);**

D\_Cache**(**mem\_blk **+** 1**)** **<=** Blk\_In**(**223 **downto** 192**);**

D\_Cache**(**mem\_blk **+** 2**)** **<=** Blk\_In**(**191 **downto** 160**);**

D\_Cache**(**mem\_blk **+** 3**)** **<=** Blk\_In**(**159 **downto** 128**);**

D\_Cache**(**mem\_blk **+** 4**)** **<=** Blk\_In**(**127 **downto** 96**);**

D\_Cache**(**mem\_blk **+** 5**)** **<=** Blk\_In**(**95 **downto** 64**);**

D\_Cache**(**mem\_blk **+** 6**)** **<=** Blk\_In**(**63 **downto** 32**);**

D\_Cache**(**mem\_blk **+** 7**)** **<=** Blk\_In**(**31 **downto** 0**);**

LW\_Done **<=** "1"**;**

**end** **if;**

--SW Hit(Address is in cache)

**elsif** **(**DHC **=** "1" and R\_W **=** "0"**)** **then**

D\_Cache**(**mem\_blk**)** **<=** Data\_In**;**

SW\_Done **<=** "1"**;**

**elsif** **(**DHC **=** "0" and R\_W **=** "0"**)** **then**

**if** **(**Blk\_In**(**255**)** **/=** 'U'**)** **then** --only does the blk replacement if a blk is inputed

D\_Cache**(**mem\_blk**)** **<=** Blk\_In**(**255 **downto** 224**);**

D\_Cache**(**mem\_blk **+** 1**)** **<=** Blk\_In**(**223 **downto** 192**);**

D\_Cache**(**mem\_blk **+** 2**)** **<=** Blk\_In**(**191 **downto** 160**);**

D\_Cache**(**mem\_blk **+** 3**)** **<=** Blk\_In**(**159 **downto** 128**);**

D\_Cache**(**mem\_blk **+** 4**)** **<=** Blk\_In**(**127 **downto** 96**);**

D\_Cache**(**mem\_blk **+** 5**)** **<=** Blk\_In**(**95 **downto** 64**);**

D\_Cache**(**mem\_blk **+** 6**)** **<=** Blk\_In**(**63 **downto** 32**);**

D\_Cache**(**mem\_blk **+** 7**)** **<=** Blk\_In**(**31 **downto** 0**);**

SW\_Done **<=** "1"**;**

**end** **if;**

**end** **if;**

**end** **if;**

**end** **process** DCache\_Proc**;**

--Look into how the memory and cache should be mapped to each other in notes

D\_Cache\_Data **<=** D\_Cache**(to\_integer(**unsigned**(**DAddr**))** mod 32**)** **after** cycle\_time **when** **(**ALU\_Done **=** "0" and DHC **=** "1" and R\_W **=** "1"**)** **else**

D\_Cache**(to\_integer(**unsigned**(**DAddr**))** mod 32**)** **after** cycle\_time **when** **(**ALU\_Done **=** "0" and DHC **=** "0" and R\_W **=** "1" and Blk\_In**(**255**)** **/=** 'U'**)** **else**

D\_Cache**(to\_integer(**unsigned**(**DAddr**))** mod 32**)** **after** cycle\_time **when** **(**ALU\_Done **=** "0" and DHC **=** "1" and R\_W **=** "0"**)** **else** --SW Hit, update mem

D\_Cache**(to\_integer(**unsigned**(**DAddr**))** mod 32**)** **after** cycle\_time **when** **(**ALU\_Done **=** "0" and DHC **=** "0" and R\_W **=** "0" and Blk\_In**(**255**)** **/=** 'U'**)** **else**

Data\_In **after** cycle\_time **when** **(**ALU\_Done **=** "0" and DHC **=** "0" and R\_W **=** "0"**);**

**end** **architecture** behave**;**

**Memory:**

--Memory: 1024 Bytes (Byte Aaddressable)

--Port Access Time: READ : 5 cycles/word

-- WRITE : 3 cycles/word

--

--Addition Time: READ : 3 cycles/word

-- WRITE : 4 cycles/word

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** IEEE**.**NUMERIC\_STD**.all;**

**entity** Memory **is**

**port** **(**Addr **:** **in** std\_logic\_vector**;** --32-bit Address between 0x0-0x3FF

IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 bit ICache Flag Input (1 for hit, 0 for miss, given by testbecnh)

DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 bit DCache Flag Input (1 for hit, 0 for miss)

R\_W **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 for read(Load), 0 for write(store)

Data\_In **:** **in** std\_logic\_vector**(**31 **downto** 0**);** --Data input used in SW Instruction

C\_type **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 for Data cache access, 0 for Instruction cache access

LW\_Done **:** **out** std\_logic\_vector**(**0 **downto** 0**);** --Load Word Done Flag

SW\_Done **:** **out** std\_logic\_vector**(**0 **downto** 0**);** --Store Word Done Flag

Data\_Out**:** **out** std\_logic\_vector**(**31 **downto** 0**);** --data output of 32-bit memory

Blk\_Out**:** **out** std\_logic\_vector**(**255 **downto** 0**));** --Block size of 8 words

**end** **entity** Memory**;**

**architecture** behave **of** Memory **is**

--initialaztion of a memory array of 1024 byte (Byte addressable decimal: 0-1023 (hex: 0x0 -> 0x3FF)

**type** array\_type **is** **array** **(**0 **to** 1023**)** **of** std\_logic\_vector**(**7 **downto** 0**);**

**signal** memory **:** array\_type **:=** **((others** **=>** **(others=>**'0'**)));** --Initialize everything to 0

**shared** **variable** mem\_blk **:** natural**;**

**signal** temp\_blk\_out**:** std\_logic\_vector**(**255 **downto** 0**);**

--Instruion Positions (addr of the instructions):

**constant** lw\_addr **:** integer **:=** 512**;** --0x200

**constant** sw\_addr **:** integer **:=** 648**;** --0x288

**constant** add\_addr **:** integer **:=** 16**;** --0x010

**constant** beq\_addr **:** integer **:=** 24**;** --0x018

**constant** bne\_addr **:** integer **:=** 32**;** --0x020

**constant** lui\_addr **:** integer **:=** 40**;** --0x028

--Cycle Time and Access time constants multipliers

**constant** cycle\_time **:** time **:=** 10 ns**;**

**constant** read\_access **:** integer **:=** 5**;**

**constant** write\_access **:** integer **:=** 3**;**

**constant** read\_add **:** integer **:=** 3**;**

**constant** write\_add **:** integer **:=** 4**;**

**begin**

mem\_proc **:** **process** **(**Addr**,** IHC**,** DHC**,** R\_W**,** Data\_In**,** C\_type**)**

**begin**

mem\_blk **:=** **to\_integer(**unsigned**(**Addr**));**

--I-Cahce Hit -> Write Thru (Write single word to memory)

**if** **(**IHC **=** "1" and C\_type **/=** "1"**)** **then**

memory**(**mem\_blk**)** **<=** Data\_In**(**31 **downto** 24**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**1**)** **<=** Data\_In**(**23 **downto** 16**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**2**)** **<=** Data\_In**(**15 **downto** 8**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**3**)** **<=** Data\_In**(**7 **downto** 0**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

--I-Cache Miss -> Write Allocate (Writes block to cache)

**elsif** **(**IHC **=** "0" and C\_type **/=** "1"**)** **then**

--Init of fake instruction memory

memory**(**lw\_addr**)** **<=** x"8D"**;**

memory**(**lw\_addr**+**1**)** **<=** x"71"**;**

memory**(**lw\_addr**+**2**)** **<=** x"00"**;**

memory**(**lw\_addr**+**3**)** **<=** x"C8"**;**

memory**(**sw\_addr**)** **<=** x"AD"**;**

memory**(**sw\_addr**+**1**)** **<=** x"93"**;**

memory**(**sw\_addr**+**2**)** **<=** x"00"**;**

memory**(**sw\_addr**+**3**)** **<=** x"64"**;**

memory**(**add\_addr**)** **<=** x"01"**;**

memory**(**add\_addr**+**1**)** **<=** x"6A"**;**

memory**(**add\_addr**+**2**)** **<=** x"90"**;**

memory**(**add\_addr**+**3**)** **<=** x"20"**;**

memory**(**beq\_addr**)** **<=** x"12"**;**

memory**(**beq\_addr**+**1**)** **<=** x"AE"**;**

memory**(**beq\_addr**+**2**)** **<=** x"01"**;**

memory**(**beq\_addr**+**3**)** **<=** x"78"**;**

memory**(**bne\_addr**)** **<=** x"16"**;**

memory**(**bne\_addr**+**1**)** **<=** x"AE"**;**

memory**(**bne\_addr**+**2**)** **<=** x"01"**;**

memory**(**bne\_addr**+**3**)** **<=** x"D4"**;**

memory**(**lui\_addr**)** **<=** x"3C"**;**

memory**(**lui\_addr**+**1**)** **<=** x"16"**;**

memory**(**lui\_addr**+**2**)** **<=** x"00"**;**

memory**(**lui\_addr**+**3**)** **<=** x"28"**;**

--D-Cache Hit -> Write Thru (Write signle word to memory)

--R\_W = 1 -> Load Branch (Outputs data at mem)

**elsif** **(**DHC **=** "1" and R\_W **=** "1" and C\_type **=** "1"**)** **then**

memory**(**mem\_blk**)** **<=** Data\_In**(**31 **downto** 24**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**1**)** **<=** Data\_In**(**23 **downto** 16**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**2**)** **<=** Data\_In**(**15 **downto** 8**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**3**)** **<=** Data\_In**(**7 **downto** 0**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

--LW\_Done <= "1" after (cycle\_time \* write\_access) + (cycle\_time \* write\_add);

--D-Cache Miss -> Write Allocate (Writes block to cache)

--R\_w = 1 -> Load Branch (Outputs blk at mem)

**elsif** **(**DHC **=** "0" and R\_W **=** "1" and C\_type **=** "1"**)** **then**

memory**(**mem\_blk**)** **<=** x"EE"**;**

memory**(**mem\_blk**+**1**)** **<=** x"EE"**;**

memory**(**mem\_blk**+**2**)** **<=** x"DD"**;**

memory**(**mem\_blk**+**3**)** **<=** x"DD"**;**

--D-Cache Hit -> Write Thru (Write single word to memory)

--R\_W = 0 -> Store Branch

**elsif** **(**DHC **=** "1" and R\_W **=** "0" and C\_type **=** "1"**)** **then**

memory**(**mem\_blk**)** **<=** Data\_In**(**31 **downto** 24**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**1**)** **<=** Data\_In**(**23 **downto** 16**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**2**)** **<=** Data\_In**(**15 **downto** 8**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**3**)** **<=** Data\_In**(**7 **downto** 0**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

--SW\_Done <= "1" after (cycle\_time \* write\_access) + (cycle\_time \* write\_add);

--D-Cache Miss -> Write Allocate (Writes block to cache)

--R\_W = 0 -> Store Word (Write word to mem, then read blks to update cache)

**elsif** **(**DHC **=** "0" and R\_W **=** "0" and C\_type **=** "1"**)** **then**

memory**(**mem\_blk**)** **<=** Data\_In**(**31 **downto** 24**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**1**)** **<=** Data\_In**(**23 **downto** 16**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**2**)** **<=** Data\_In**(**15 **downto** 8**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

memory**(**mem\_blk**+**3**)** **<=** Data\_In**(**7 **downto** 0**)** **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**);**

**end** **if;**

**end** **process** mem\_proc**;**

--Writing the blk into the temp\_blk

temp\_blk\_out**(**255 **downto** 224**)** **<=** memory**(**mem\_blk**)** **&** memory**(**mem\_blk **+** 1**)** **&** memory**(**mem\_blk **+** 2**)** **&** memory**(**mem\_blk **+** 3**);**

temp\_blk\_out**(**223 **downto** 192**)** **<=** memory**(**mem\_blk **+** 4**)** **&** memory**(**mem\_blk **+** 5**)** **&** memory**(**mem\_blk **+** 6**)** **&** memory**(**mem\_blk **+** 7**);**

temp\_blk\_out**(**191 **downto** 160**)** **<=** memory**(**mem\_blk **+** 8**)** **&** memory**(**mem\_blk **+** 9**)** **&** memory**(**mem\_blk **+** 10**)** **&** memory**(**mem\_blk **+** 11**);**

temp\_blk\_out**(**159 **downto** 128**)** **<=** memory**(**mem\_blk **+** 12**)** **&** memory**(**mem\_blk **+** 13**)** **&** memory**(**mem\_blk **+** 14**)** **&** memory**(**mem\_blk **+** 15**);**

temp\_blk\_out**(**127 **downto** 96**)** **<=** memory**(**mem\_blk **+** 16**)** **&** memory**(**mem\_blk **+** 17**)** **&** memory**(**mem\_blk **+** 18**)** **&** memory**(**mem\_blk **+** 19**);**

temp\_blk\_out**(**95 **downto** 64**)** **<=** memory**(**mem\_blk **+** 20**)** **&** memory**(**mem\_blk **+** 21**)** **&** memory**(**mem\_blk **+** 22**)** **&** memory**(**mem\_blk **+** 23**);**

temp\_blk\_out**(**63 **downto** 32**)** **<=** memory**(**mem\_blk **+** 24**)** **&** memory**(**mem\_blk **+** 25**)** **&** memory**(**mem\_blk **+** 26**)** **&** memory**(**mem\_blk **+** 27**);**

temp\_blk\_out**(**31 **downto** 0**)** **<=** memory**(**mem\_blk **+** 28**)** **&** memory**(**mem\_blk **+** 29**)** **&** memory**(**mem\_blk **+** 30**)** **&** memory**(**mem\_blk **+** 31**);**

--When IHC = 1, write Data Out

Data\_Out **<=** Data\_In **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**)** **when** **(**IHC **=** "1" and C\_type **/=** "1"**)** **else**

Data\_In **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**)** **when** **(**DHC **=** "1" and R\_W **=** "1" and C\_type **=** "1"**)** **else**

Data\_In **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**)** **when** **(**DHC **=** "0" and R\_W **=** "0" and C\_type **=** "1"**);**

--When IHC = 0, write Blk\_Out

Blk\_Out **<=** temp\_blk\_out **after** 8**\*((**cycle\_time **\*** read\_access**)** **+** **(**cycle\_time **\*** read\_add**))** **when** **(**IHC **=** "0" and C\_type **/=** "1"**)** **else**

temp\_blk\_out **after** 8**\*((**cycle\_time **\*** read\_access**)** **+** **(**cycle\_time **\*** read\_add**))** **when** **(**DHC **=** "0" and R\_W **=** "1" and C\_type **=** "1"**)** **else**

temp\_blk\_out **after** 8**\*((**cycle\_time **\*** read\_access**)** **+** **(**cycle\_time **\*** read\_add**))** **when** **(**DHC **=** "0" and R\_W **=** "0" and C\_type **=** "1"**);**

LW\_Done **<=** "1" **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**)** **when** **(**DHC **=** "1" and R\_W **=** "1" and C\_type **=** "1"**)** **else**

"1" **after** **(**8**\*((**cycle\_time **\*** read\_access**)** **+** **(**cycle\_time **\*** read\_add**)))** **when** **(**DHC **=** "0" and R\_W **=** "1" and C\_type **=** "1"**);**

SW\_Done **<=** "1" **after** **(**cycle\_time **\*** write\_access**)** **+** **(**cycle\_time **\*** write\_add**)** **when** **(**DHC **=** "1" and R\_W **=** "0" and C\_type **=** "1"**)** **else**

"1" **after** **(**8**\*((**cycle\_time **\*** read\_access**)** **+** **(**cycle\_time **\*** read\_add**)))** **when** **(**DHC **=** "0" and R\_W **=** "0" and C\_type **=** "1"**)** **;**

**end** **architecture** behave**;**

**CPU:**

--CPU:

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** IEEE**.**NUMERIC\_STD**.all;**

**use** ieee**.**numeric\_std**.all;**

**use** ieee**.**std\_logic\_arith**.all;**

**entity** CPU **is**

**port** **(**OPC **:** **in** std\_logic\_vector**(**31 **downto** 0**);**--OP code for instruction

ALU\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

R\_W**:** **out** std\_logic\_vector **(**0 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

DAddr**:** **out** std\_logic\_vector **(**31 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

Data**:** **out** std\_logic\_vector **(**0 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

Data\_reg**:** **out** std\_logic\_vector **(**31 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

Reg\_Num**:** **out** std\_logic\_vector **(**4 **downto** 0**));** --5 bit register number

**end** **entity** CPU**;**

**architecture** behave **of** CPU **is**

**begin**

OPC\_Proc **:** **process** **(**OPC**)**

**begin**

-- Check type of instruction

**if** **(**OPC **=** x"8D7100C8"**)** **then** --Load instruction

**report** "In load"**;**

ALU\_DONE**<=**"0"**;**

DAddr**<=**x"000000D9"**;** --200 + $11

R\_W**<=**"1"**;**

Data**<=**"1"**;**

Data\_reg**<=**x"00000000"**;**

Reg\_Num **<=** "10001"**;** --R17

**elsif** **(**OPC **=** x"AD930064"**)** **then** -- Store instruction

**report** "In Store"**;**

ALU\_DONE**<=**"0"**;**

DAddr**<=**x"00000076"**;** --100 + $12

R\_W**<=**"0"**;**

Data**<=**"1"**;**

Data\_reg**<=**x"00000019"**;**

**elsif** **(**OPC **=** x"016A9020"**)** **then** --Add

ALU\_DONE**<=**"1"**;**

DAddr**<=**x"00000000"**;**

Data**<=**"0"**;**

Data\_reg**<=**x"00000000"**;**

Reg\_Num **<=** "10011"**;**

**elsif** **(**OPC **=** x"3C160028"**)** **then** --LUI

ALU\_DONE**<=**"1"**;**

DAddr**<=**x"00000000"**;**

Data**<=**"0"**;**

Data\_reg**<=**x"00000000"**;**

Reg\_Num **<=** "10110"**;**

**else** --ALU instruction

**report** "In ALU"**;**

ALU\_DONE**<=**"1"**;**

DAddr**<=**x"00000000"**;**

Data**<=**"0"**;**

Data\_reg**<=**x"00000000"**;**

Reg\_Num **<=** "00000"**;**

**end** **if;**

**end** **process** OPC\_Proc**;**

**end** **architecture** behave**;**

**BUS:**

--Bus: Used to transfer words and blocks between cahce and memeory.

--Bandwidth of 32words/cycle

--Assume that the bw will never be exceeded and will always take

--up the full cycle

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** Bus\_Model **is**

**port** **(**Addr **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

IHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

DHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

R\_W **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

C\_Type **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

Data\_In **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

Blk\_In **:** **in** std\_logic\_vector **(**255 **downto** 0**);**

Addr\_Out**:** **out** std\_logic\_vector **(**31 **downto** 0**);**

IHC\_Out**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

DHC\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

R\_W\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

C\_Type\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

Data\_Out **:** **out** std\_logic\_vector **(**31 **downto** 0**);**

Blk\_Out **:** **out** std\_logic\_vector**(**255 **downto** 0**));**

**end** **entity** Bus\_Model**;**

**architecture** behave **of** Bus\_Model **is**

**constant** cycle\_time **:** time **:=** 10 ns**;**

**begin**

Addr\_Out **<=** Addr **after** cycle\_time**;**

IHC\_Out **<=** IHC **after** cycle\_time**;**

DHC\_Out **<=** DHC **after** cycle\_time**;**

R\_W\_Out **<=** R\_W **after** cycle\_time**;**

C\_Type\_Out **<=** C\_Type **after** cycle\_time**;**

Data\_Out **<=** Data\_In **after** cycle\_time**;**

Blk\_Out **<=** Blk\_In **after** cycle\_time**;**

**end** **architecture** behave**;**

**MUX2\_32:**

--MUX FOR 2-input 32-bit Information

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** Mux2\_32 **is**

**port** **(**ZERO**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

ONE**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

CTRL**:** **in** std\_logic\_vector**(**0 **downto** 0**);**

OUTPUT**:** **out** std\_logic\_vector**(**31 **downto** 0**));**

**end** **entity** Mux2\_32**;**

**architecture** behavior **of** Mux2\_32 **is**

**begin**

OUTPUT **<=** ONE **when** **(**CTRL **=** "1"**)** **else** --I-TYPE, Outputs IMM

ZERO**;**

**end** **architecture** behavior**;**

**MUX22\_32:**

--MUX FOR 2-input 32-bit Information with 2x1-bit control

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** Mux22\_32 **is**

**port** **(**ZERO**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

ONE**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

CTRL1**:** **in** std\_logic\_vector**(**0 **downto** 0**);**

CTRL2**:** **in** std\_logic\_vector **(**0 **downto** 0**);**

OUTPUT**:** **out** std\_logic\_vector**(**31 **downto** 0**));**

**end** **entity** Mux22\_32**;**

**architecture** behavior **of** Mux22\_32 **is**

**begin**

OUTPUT **<=** ONE **when** **(**CTRL1 **=** "1" and CTRL2 **=** "1"**)** **else** --I-TYPE, Outputs IMM

ZERO **when** **(**CTRL1 **=** "0" and CTRL2 **=** "1"**);**

**end** **architecture** behavior**;**

**Register\_Data:**

--Register\_Data

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**numeric\_std**.all;**

**entity** Register\_Data **is**

**port** **(**Reg\_Num**:** **in** std\_logic\_vector**(**4 **downto** 0**);** --5-bit Read Reg. 1

Data\_In**:** **in** std\_logic\_vector**(**31 **downto** 0**));**

**end** **entity** Register\_Data**;**

**architecture** behave **of** Register\_Data **is**

--Changing Vectors

**signal** REG\_8**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000008"**;**

**signal** REG\_9**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000009"**;**

**signal** REG\_10**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000010"**;**

**signal** REG\_11**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000011"**;**

**signal** REG\_12**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000012"**;**

**signal** REG\_13**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000013"**;**

**signal** REG\_14**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000014"**;**

**signal** REG\_15**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000015"**;**

**signal** REG\_16**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000016"**;**

**signal** REG\_17**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000017"**;**

**signal** REG\_18**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000018"**;**

**signal** REG\_19**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000019"**;**

**signal** REG\_20**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000020"**;**

**signal** REG\_21**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000021"**;**

**signal** REG\_22**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000022"**;**

**signal** REG\_23**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000023"**;**

**signal** REG\_24**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000024"**;**

**signal** REG\_25**:** std\_logic\_vector**(**31 **downto** 0**)** **:=** x"00000025"**;**

**begin**

Reg\_19 **<=** x"00000021" **when** Reg\_Num **=** "10011"**;** --simulated addition

Reg\_22 **<=** x"00280022" **when** Reg\_Num **=** "10110"**;** --simulated lui

Reg\_17 **<=** Data\_In **when** Reg\_num **=** "10001"**;** --sumulates lw

**end** **architecture** behave**;**

**ICache\_Dataflow:**

--BETA Class for the instruction cache,mem and CPU process

--NOTE:ADD bus

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**numeric\_std**.all;**

**entity** ICache\_Dataflow **is**

**port** **(**aIAddr **:** **in** std\_logic\_vector**(**31 **downto** 0**);**

aIHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

aALU\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aR\_W**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aDAddr**:** **out** std\_logic\_vector **(**31 **downto** 0**);**

aData**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aData\_reg**:** **out** std\_logic\_vector **(**31 **downto** 0**);**

aReg\_Num**:** **out** std\_logic\_vector **(**4 **downto** 0**));** --5 bit register number

**end** ICache\_Dataflow**;**

**architecture** behave **of** ICache\_Dataflow **is**

**COMPONENT** I\_Cache **is**

**port** **(**IAddr **:** **in** std\_logic\_vector**;** -- 0x0 - 0x40

IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

Blk\_In**:** **in** std\_logic\_vector**(**255 **downto** 0**);** --Block size of 8 words

I\_Cache\_Data**:** **out** std\_logic\_vector**(**31 **downto** 0**));** --data output of 32-bit memory

**end** **COMPONENT;**

**COMPONENT** Mux2\_32 **is**

**port** **(**ZERO**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

ONE**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

CTRL**:** **in** std\_logic\_vector**(**0 **downto** 0**);**

OUTPUT**:** **out** std\_logic\_vector**(**31 **downto** 0**));**

**end** **COMPONENT;**

**COMPONENT** Memory **is**

**port** **(**Addr **:** **in** std\_logic\_vector**;** --32-bit Address between 0x0-0x3FF

IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 bit ICache Flag Input (1 for hit, 0 for miss, given by testbecnh)

DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 bit DCache Flag Input (1 for hit, 0 for miss)

R\_W **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 for read(Load), 0 for write(store)

Data\_In **:** **in** std\_logic\_vector**(**31 **downto** 0**);**-- Data input used in SW Instruction

C\_type **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 for Data cache access, 0 for Instruction cache access

LW\_Done **:** **out** std\_logic\_vector**(**0 **downto** 0**);**

SW\_Done **:** **out** std\_logic\_vector**(**0 **downto** 0**);**

Data\_Out**:** **out** std\_logic\_vector**(**31 **downto** 0**);** --data output of 32-bit memory

Blk\_Out**:** **out** std\_logic\_vector**(**255 **downto** 0**));** --Block size of 8 words

**end** **COMPONENT;**

**COMPONENT** CPU **is**

**port** **(**OPC **:** **in** std\_logic\_vector**(**31 **downto** 0**);**--OP code for instruction

ALU\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

R\_W**:** **out** std\_logic\_vector **(**0 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

DAddr**:** **out** std\_logic\_vector **(**31 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

Data**:** **out** std\_logic\_vector **(**0 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

Data\_reg**:** **out** std\_logic\_vector **(**31 **downto** 0**);** --2 bit Instruction type flag (0==Load) (1==Store) (2==Alu)

Reg\_Num**:** **out** std\_logic\_vector **(**4 **downto** 0**));** --5 bit register number

**end** **COMPONENT;**

**COMPONENT** Bus\_Model **is**

**port** **(**Addr **:** **in** std\_logic\_vector**;**

IHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

DHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

R\_W **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

C\_Type **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

Data\_In **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

Blk\_In **:** **in** std\_logic\_vector **(**255 **downto** 0**);**

Addr\_Out**:** **out** std\_logic\_vector**;**

IHC\_Out**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

DHC\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

R\_W\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

C\_Type\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

Data\_Out **:** **out** std\_logic\_vector **(**31 **downto** 0**);**

Blk\_Out **:** **out** std\_logic\_vector**(**255 **downto** 0**));**

**end** **COMPONENT;**

------------------------------------------------First Cache Signals------------------------------------------------------

--Declaration of Inputs

**signal** ICACHE\_I\_IAddr **:** std\_logic\_vector **(**7 **downto** 0**);**

**signal** ICACHE\_I\_IHC **:** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag

**signal** ICACHE\_I\_Blk\_In**:** std\_logic\_vector**(**255 **downto** 0**);**

--Declaration of Outputs

**signal** ICACHE\_I\_I\_Cache\_Data**:** std\_logic\_vector**(**31 **downto** 0**);**

------------------------------------------------Second Cache Signals------------------------------------------------------

--Declaration of Inputs

**signal** ICACHE\_II\_IAddr **:** std\_logic\_vector **(**7 **downto** 0**);**

**signal** ICACHE\_II\_IHC **:** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag

**signal** ICACHE\_II\_Blk\_In**:** std\_logic\_vector**(**255 **downto** 0**);** --1 for read, 0 for write

--Declaration of Outputs

**signal** ICACHE\_II\_cache\_Data**:** std\_logic\_vector**(**31 **downto** 0**);**

------------------------------------------------Memory Signals------------------------------------------------------------

--Declaration of test signal Inputs

**signal** MEM\_Addr **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** MEM\_IHC **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** MEM\_DHC **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** MEM\_R\_W **:** std\_logic\_vector**(**0 **downto** 0**);** --1 for read, 0 for write

**signal** MEM\_Data\_In **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** MEM\_C\_type **:** std\_logic\_vector**(**0 **downto** 0**);**

--Declaration of test signal Outputs

**signal** MEM\_LW\_Done **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** MEM\_SW\_Done **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** MEM\_Data\_Out**:** std\_logic\_vector**(**31 **downto** 0**);** --data output of 32-bit MEM

**signal** MEM\_Blk\_Out**:** std\_logic\_vector**(**255 **downto** 0**);** --Block size of 8 words

------------------------------------------------Mux Signals---------------------------------------------------------------

--Declaration of test signal Inputs

**signal** MUX\_ZERO**:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** MUX\_ONE**:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** MUX\_CTRL**:** std\_logic\_vector**(**0 **downto** 0**);**

--Declaration of test signal Outputs

**signal** MUX\_OUTPUT**:** std\_logic\_vector**(**31 **downto** 0**);**

------------------------------------------------CPU Signals---------------------------------------------------------------

--Declaration of test signal Inputs

**signal** CPU\_OPC **:** std\_logic\_vector**(**31 **downto** 0**);**

--Declaration of test signal Outputs

**signal** CPU\_ALU\_DONE**:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** CPU\_R\_W**:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** CPU\_DAddr**:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** CPU\_Data**:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** CPU\_Data\_reg**:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** T\_Addr\_Out **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** T\_Data\_out **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** T\_Data\_out2 **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** T\_Data\_out3 **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** T\_Data\_out4 **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** T\_Blk\_Out2 **:** std\_logic\_vector**(**255 **downto** 0**);**

**begin**

i\_cache\_1**:** I\_Cache **PORT** **MAP** **(**

IAddr**=>**aIAddr**,**

IHC **=>**aIHC**,**

Blk\_In **=>**T\_Blk\_Out2**,** --in (Undriven for first cache)

I\_Cache\_Data **=>**T\_Data\_out**);**

Bus\_1 **:** Bus\_Model **port** **map** **(**Addr **=>** aIAddr**,**

IHC **=>** aIHC**,**

DHC **=>** "U"**,**

R\_W **=>** "U"**,**

C\_Type **=>** "0"**,**

Data\_In **=>** T\_Data\_out**,**

Blk\_In **=>** MEM\_Blk\_Out**,**

Addr\_Out **=>**T\_Addr\_Out**,**

Data\_Out **=>** T\_Data\_Out2**);**

mem**:** Memory **PORT** **MAP** **(**

Addr **=>** aIAddr**,**--in

IHC **=>** aIHC**,** --in

DHC **=>** "U"**,** --in (Undriven for Instruction flow)

R\_W **=>** "U"**,** --in (Undriven for Instruction flow)

Data\_In **=>** T\_Data\_Out2**,**--in

C\_type **=>** "0"**,** --in (instruction)

--LW\_Done => "0", --(Undriven for Instruction flow)

--SW\_Done => "0", --(Undriven for Instruction flow)

Data\_Out **=>** T\_Data\_out3**,** --(Undriven for Instruction flow)

Blk\_Out **=>** MEM\_Blk\_Out**);**

Bus\_2 **:** Bus\_Model **port** **map** **(**Addr **=>** aIAddr**,**

IHC **=>** aIHC**,**

DHC **=>** "U"**,**

R\_W **=>** "U"**,**

C\_Type **=>** "0"**,**

Data\_In **=>** T\_Data\_out3**,**

Blk\_In **=>** MEM\_Blk\_Out**,**

Addr\_Out **=>**T\_Addr\_Out**,**

Data\_Out **=>** T\_Data\_Out4**,**

Blk\_Out **=>** T\_Blk\_Out2**);**

-- i\_cache\_2: I\_Cache PORT MAP (

-- IAddr=>aIAddr,--in

-- IHC => aIHC,--in

-- Blk\_In => MEM\_Blk\_Out,--in

-- I\_Cache\_Data =>ICACHE\_II\_Cache\_Data);

mux**:** Mux2\_32 **PORT** **MAP** **(**

ZERO **=>** T\_Data\_out**,** --in

ONE **=>** T\_Data\_Out4**,**--in

CTRL **=>** aIHC**,**--in

OUTPUT **=>** MUX\_OUTPUT**);**

cpu\_uut**:** CPU **PORT** **MAP** **(**

OPC **=>** MUX\_OUTPUT**,** --in

ALU\_DONE **=>** aALU\_DONE**,**

R\_W **=>** aR\_W**,**

DAddr **=>** aDAddr**,**

Data **=>** aData**,**

Data\_reg **=>** aData\_reg**,**

Reg\_Num**=>**aReg\_Num**);**

**end** **architecture** behave**;**

**DCache Dataflow:**

--Combination of DCache, Mem

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** DCache\_Dataflow **is**

**port** **(**aDAddr **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

aData **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

aBlk **:** **in** std\_logic\_vector **(**255 **downto** 0**);**

aALU\_Done **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aR\_W **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aDHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aType **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aOut **:** **out** std\_logic\_vector **(**31 **downto** 0**);**

aLW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aSW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**));**

**end** **entity** DCache\_Dataflow**;**

**architecture** behave **of** DCache\_Dataflow **is**

--Component declaration

**COMPONENT** D\_Cache **is**

**port** **(**DAddr **:** **in** std\_logic\_vector**;** --Data address

DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 bit DCache Flag Input (1 for hit, 0 for miss, given by testbecnh)

Data\_In **:** **in** std\_logic\_vector**(**31 **downto** 0**);** --32-bit data in

Blk\_In**:** **in** std\_logic\_vector**(**255 **downto** 0**);** --Block size of 8 words

R\_W **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 for load, 0 for store

ALU\_Done **:** **in** std\_logic\_vector **(**0 **downto** 0**);** --1 for done, 0 for not done

LW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**);** --1 for done, 0 for not done

SW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**);** --1 for done, 0 for not done

D\_Cache\_Data**:** **out** std\_logic\_vector**(**31 **downto** 0**));** --data output of 32-bit memory

**end** **COMPONENT;**

**COMPONENT** Bus\_Model **is**

**port** **(**Addr **:** **in** std\_logic\_vector**;**

IHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

DHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

R\_W **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

C\_Type **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

Data\_In **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

Blk\_In **:** **in** std\_logic\_vector **(**255 **downto** 0**);**

Addr\_Out**:** **out** std\_logic\_vector**;**

IHC\_Out**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

DHC\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

R\_W\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

C\_Type\_Out **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

Data\_Out **:** **out** std\_logic\_vector **(**31 **downto** 0**);**

Blk\_Out **:** **out** std\_logic\_vector**(**255 **downto** 0**));**

**end** **COMPONENT;**

**COMPONENT** Memory **is**

**port** **(**Addr **:** **in** std\_logic\_vector**;** --32-bit Address between 0x0-0x3FF

IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 bit ICache Flag Input (1 for hit, 0 for miss, given by testbecnh)

DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** -- 1 bit DCache Flag Input (1 for hit, 0 for miss)

R\_W **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 for read(Load), 0 for write(store)

Data\_In **:** **in** std\_logic\_vector**(**31 **downto** 0**);**-- Data input used in SW Instruction

C\_type **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --1 for Data cache access, 0 for Instruction cache access

LW\_Done **:** **out** std\_logic\_vector**(**0 **downto** 0**);**

SW\_Done **:** **out** std\_logic\_vector**(**0 **downto** 0**);**

Data\_Out**:** **out** std\_logic\_vector**(**31 **downto** 0**);** --data output of 32-bit memory

Blk\_Out**:** **out** std\_logic\_vector**(**255 **downto** 0**));** --Block size of 8 words

**end** **COMPONENT;**

**COMPONENT** Mux22\_32 **is**

**port** **(**ZERO**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

ONE**:** **in** std\_logic\_vector**(**31 **downto** 0**);**

CTRL1**:** **in** std\_logic\_vector**(**0 **downto** 0**);**

CTRL2**:** **in** std\_logic\_vector**(**0 **downto** 0**);**

OUTPUT**:** **out** std\_logic\_vector**(**31 **downto** 0**));**

**end** **COMPONENT;**

--Temp signals used as connections between components

**signal** T\_Data\_In **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** T\_Blk\_In **:** std\_logic\_vector **(**255 **downto** 0**);**

**signal** T\_Data\_Out **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** T\_Data\_Out2 **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** T\_Data\_Out3 **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** T\_Data\_Out4 **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** T\_Blk\_Out **:** std\_logic\_vector **(**255 **downto** 0**);**

**signal** T\_Blk\_Out2 **:** std\_logic\_vector **(**255 **downto** 0**);**

**signal** T\_Addr\_Out **:** std\_logic\_vector**(**31 **downto** 0**);**

**begin**

D\_Cache\_Mod **:** D\_Cache **port** **map** **(**DAddr **=>** aDAddr**,**

DHC **=>** aDHC**,**

Data\_In **=>** aData**,**

Blk\_In **=>** T\_Blk\_Out2**,**

R\_W **=>** aR\_W**,**

ALU\_Done **=>** aALU\_Done**,**

LW\_Done **=>** aLW\_Done**,**

SW\_Done **=>** aSW\_Done**,**

D\_Cache\_Data **=>** T\_Data\_Out**);**

Bus\_1 **:** Bus\_Model **port** **map** **(**Addr **=>** aDAddr**,**

IHC **=>** "U"**,**

DHC **=>** aDHC**,**

R\_W **=>** aR\_W**,**

C\_Type **=>** aType**,**

Data\_In **=>** T\_Data\_Out**,**

Blk\_In **=>** aBlk**,**

Addr\_Out **=>**T\_Addr\_Out**,**

Data\_Out **=>** T\_Data\_Out2**);**

D\_Mem **:** Memory **port** **map** **(**Addr **=>** aDAddr**,**

IHC **=>** "U"**,**

DHC **=>** aDHC**,**

R\_W **=>** aR\_W**,**

Data\_In **=>** T\_Data\_Out2**,**

C\_type **=>** aType**,**

LW\_Done **=>** aLW\_Done**,**

SW\_Done **=>** aSW\_Done**,**

Data\_Out **=>** T\_Data\_Out3**,**

Blk\_Out **=>** T\_Blk\_Out**);**

Bus\_2 **:** Bus\_Model **port** **map** **(**Addr **=>** aDAddr**,**

IHC **=>** "U"**,**

DHC **=>** aDHC**,**

R\_W **=>** aR\_W**,**

C\_Type **=>** aType**,**

Data\_In **=>** T\_Data\_Out3**,**

Blk\_In **=>** T\_Blk\_Out**,**

Addr\_Out **=>**T\_Addr\_Out**,**

Data\_Out **=>** T\_Data\_Out4**,**

Blk\_Out **=>** T\_Blk\_Out2**);**

Mux\_32 **:** Mux22\_32 **port** **map** **(**ZERO **=>** T\_Data\_Out**,**

ONE **=>** T\_Data\_Out4**,**

CTRL1 **=>** aDHC**,**

CTRL2 **=>** aR\_W**,**

OUTPUT **=>** aOut**);**

**end** **architecture** behave**;**

**Cache\_Memory\_Dataflow:**

--BETA Class for the instruction cache,mem and CPU process

--NOTE:ADD bus

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**use** ieee**.**numeric\_std**.all;**

**entity** Cache\_Memory\_Dataflow **is**

**port** **(**t\_IAddr **:** **in** std\_logic\_vector**(**31 **downto** 0**);**

t\_IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

t\_DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);**

t\_ALU\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

t\_LW\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

t\_SW\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

t\_Data\_Out**:** **out** std\_logic\_vector **(**31 **downto** 0**));** --5 bit register number

**end** Cache\_Memory\_Dataflow**;**

**architecture** behave **of** Cache\_Memory\_Dataflow **is**

**COMPONENT** ICache\_Dataflow **is**

**port** **(**aIAddr **:** **in** std\_logic\_vector**(**31 **downto** 0**);**

aIHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

aALU\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aR\_W**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aDAddr**:** **out** std\_logic\_vector **(**31 **downto** 0**);**

aData**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aData\_reg**:** **out** std\_logic\_vector **(**31 **downto** 0**);**

aReg\_Num**:** **out** std\_logic\_vector **(**4 **downto** 0**));** --5 bit register number

**end** **component;**

**COMPONENT** DCache\_Dataflow **is**

**port** **(**aDAddr **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

aData **:** **in** std\_logic\_vector **(**31 **downto** 0**);**

aBlk **:** **in** std\_logic\_vector **(**255 **downto** 0**);**

aALU\_Done **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aR\_W **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aDHC **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aType **:** **in** std\_logic\_vector **(**0 **downto** 0**);**

aOut **:** **out** std\_logic\_vector **(**31 **downto** 0**);**

aLW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**);**

aSW\_Done **:** **out** std\_logic\_vector **(**0 **downto** 0**));**

**end** **component;**

**COMPONENT** Register\_Data **is**

**port** **(**Reg\_Num**:** **in** std\_logic\_vector **(**4 **downto** 0**);** --5-bit Read Reg. 1

Data\_In**:** **in** std\_logic\_vector **(**31 **downto** 0**));**

**end** **component;**

**signal** temp\_rw **:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** temp\_DAddr **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** temp\_C\_Type **:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** temp\_CPU\_Data **:** std\_logic\_vector **(**31 **downto** 0**);**

**signal** temp\_Reg\_Num **:** std\_logic\_vector **(**4 **downto** 0**);**

**signal** not\_used\_in\_this\_test **:** std\_logic\_vector **(**255 **downto** 0**);**

**signal** temp\_ALU\_DONE **:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** temp\_Data\_Out **:** std\_logic\_vector **(**31 **downto** 0**);**

**begin**

ICache **:** ICache\_Dataflow **port** **map(**aIAddr **=>** t\_IAddr**,**

aIHC **=>** t\_IHC**,**

aALU\_DONE **=>** temp\_ALU\_DONE**,**

aR\_W **=>** temp\_rw**,**

aDAddr **=>** temp\_DAddr**,**

aData **=>** temp\_C\_Type**,**

aData\_reg **=>** temp\_CPU\_Data**,**

aReg\_Num **=>** temp\_Reg\_Num**);**

DCache **:** DCache\_Dataflow **port** **map(**aDAddr **=>** temp\_DAddr**,**

aData **=>** temp\_CPU\_Data**,**

aBlk **=>** not\_used\_in\_this\_test**,**

aALU\_Done **=>** temp\_ALU\_DONE**,**

aR\_W **=>** temp\_rw**,**

aDHC **=>** t\_DHC**,**

aType **=>** temp\_C\_Type**,**

aOut **=>** temp\_Data\_Out**,**

aLW\_Done **=>** t\_LW\_DONE**,**

aSW\_Done **=>** t\_SW\_DONE**);**

Reg\_File **:** Register\_Data **port** **map(**Reg\_Num **=>** temp\_Reg\_Num**,**

Data\_In **=>** temp\_Data\_Out**);**

t\_ALU\_DONE **<=** temp\_ALU\_DONE**;**

t\_Data\_Out **<=** temp\_Data\_Out**;**

**end** **architecture** behave**;**

**Cache\_Memory\_Dataflow\_Test (Overall Testbench Program):**

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** Cache\_Memory\_Dataflow\_Test **is**

**end** **entity;**

**architecture** behave **of** Cache\_Memory\_Dataflow\_Test **is**

**COMPONENT** Cache\_Memory\_Dataflow **is**

**port** **(**t\_IAddr **:** **in** std\_logic\_vector**(**31 **downto** 0**);**

t\_IHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

t\_DHC **:** **in** std\_logic\_vector**(**0 **downto** 0**);**

t\_ALU\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

t\_LW\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

t\_SW\_DONE**:** **out** std\_logic\_vector **(**0 **downto** 0**);**

t\_Data\_Out**:** **out** std\_logic\_vector **(**31 **downto** 0**));** --5 bit register number

**end** **COMPONENT;**

--Declaration of test signal Inputs

**signal** TB\_aIAddr **:** std\_logic\_vector**(**31 **downto** 0**);**

**signal** TB\_aIHC **:** std\_logic\_vector**(**0 **downto** 0**);** --I-Cahche hit flag 1: Hit 0: Miss

**signal** TB\_aDHC **:** std\_logic\_vector**(**0 **downto** 0**);** --D-Cahche hit flag 1: Hit 0: Miss

--Declaration of test signal Outputs

**signal** TB\_ALU\_DONE**:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** TB\_LW\_DONE**:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** TB\_SW\_DONE**:** std\_logic\_vector **(**0 **downto** 0**);**

**signal** TB\_Data\_Out**:** std\_logic\_vector **(**31 **downto** 0**);**

**begin**

uut**:** Cache\_Memory\_Dataflow **PORT** **MAP** **(**

t\_IAddr**=>**TB\_aIAddr**,**

t\_IHC **=>** TB\_aIHC**,**

t\_DHC **=>** TB\_aDHC**,**

t\_ALU\_DONE**=>** TB\_ALU\_DONE**,**

t\_LW\_DONE**=>** TB\_LW\_DONE**,**

t\_SW\_DONE**=>** TB\_SW\_DONE**,**

t\_Data\_Out**=>**TB\_Data\_Out**);**

aAddr\_Gen **:** **process**

**begin**

TB\_aIAddr **<=** --x"00000200" after 0 ns; --Load Address

x"00000288" **after** 0 ns**;** --Store Address

-- x"00000010" after 0 ns; --Add Address

-- x"00000018" after 0 ns; --BEQ Address

-- x"00000020" after 0 ns; --BNE Address

-- x"00000028" after 0 ns; --LUI Address

**wait;**

**end** **process** aAddr\_Gen**;**

aIHC\_Gen **:** **process**

**begin**

TB\_aIHC **<=** "1" **after** 0 ns**;** --ICache Hit

--"0" after 0 ns; --ICache Miss

**wait;**

**end** **process** aIHC\_Gen**;**

aDHC\_Gen **:** **process**

**begin**

TB\_aDHC **<=** --"1" after 0 ns; --DCache Hit

"0" **after** 0 ns**;** --DCache Miss

**wait;**

**end** **process** aDHC\_Gen**;**

**end** **architecture** behave**;**